

SynthWorks

VHDL Training Solutions for hardware design and test.

Synopsys Synplify Quick Reference

1. Steps to Synthesis

Start the Synthesis Tool
Create a Project
Order the Files in the Project
Save the Project
Pre-Compile the Design
Set Constraints
Select Target Technology
Synthesis the Design
View the Design
Check Timing

These steps are enumerated below.

2. Start the Synthesis Tool

Windows: Select Synplicity Simplify from start menu or desktop

Hint: On the shortcut to Synplify, set the Start In field to your lab working directory.

3. Create a Project

Menu: File> Build Project

In the GUI box,

- 1) Navigate to the directory
- 2) Select Design File(s)
- 3) Press Add to add the file(s) to the project
- 4) Press OK.

4. Re-order the Files in the Project

If the VHDL directory is not open in the project window, click on the plus sign (+) to open it. If the top of your design is not last, drag it and make it last.

5. Save the Project

Menu: File> Save

6. Pre-Compile the Design

Menu: Run > Compile Only

This is preparation for setting constraints. Can't set constraints unless tool knows signals in the design.

7. Set Constraints

Menu: File > New

In multiple pop-up boxes:

Box 1: Select Constraints File (Scope)

Box 2: Initialize constraints, select all (default) and press ok

In the constraints box, select the Clocks tab (along the bottom) and set the clock frequency. Make sure to check the box to the left of the clock value.

In the constraints box, select the Inputs/Outputs tab and set a value for <input default> and <output default>. Make sure to check the box next to the left of these fields.

Now save the constraints file by doing a "file > Save" from the menu.

8. Select Target Technology

Menu: Project > Implementation Options

Under the following tabs do the following:

Device: Select Device

Options: Select constraint file

Timing Reports: Number of Critical Paths = 25

When you are done, click ok.

9. Synthesize the Design

Project Window: RUN

Results are ready when tool displays DONE

10. View the Design (RTL Netlist)

Menu: HDL Analyst > RTL > Hierarchical Vi

Tool Bar / Buttons: Click on "+" sign = Adder Symbol

11. Check Timing

Project Window: View Log

Log file has compile messages (warnings, errors), and timing and device information.

12. Changing Between Labs

Select VHDL file. Right-click and select change file. No need to create a new project.

13. Adding Files

Menu: Project > Add Source File ...

Left Tool Bar: Add File ...

14. Setting the Library

Under VHDL, select the file, right click and select "File Options", under library name enter the library name (such as ieee_proposed).

15. Help on Synplify

Menu: Help > Online Documents

Make sure to do this with the project window selected.

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