Intermediate VHDL for Synthesis and Verification

3-5 Days: 50% lecture, 50% Lab Intermediate Level

Overview
Course materials come from the following core courses:
- Intermediate VHDL Coding Styles for Synthesis (2 days)
- VHDL Testbenches and Verification (3 days)

Course Outline
The full 5 day outline is as follows:

Day 1, Synthesis Module Syn1
- Synthesis Overview
- Combinational Logic
- Registers and Latches
- UART Transmitter:
  - RTL Code + Statemachine

Day 2, Synthesis Module Syn2
- Numeric Types and Packages
- Arithmetic Logic
- Comparison and Multiplication
- Partitioning
- Synthesis Process

Day 3, Testbench Module Tb1
- Testbench Overview
- Basic Testbenches
- Transactions and Subprograms
- Modeling for Verification
- VHDL IO

Day 4, Testbench Module Tb2
- Lab Review: Testing w/ subprograms
- Transaction-Based BFM
- Execution and Timing
- Elements of a Transaction-Based BFM

Day 5, Testbench Module Tb3
- Configurations and Simulation Management
- From Subblock to System Tests
- Creating Tests
- Modeling RAM

Customization Possibilities
- 4 Day Class: Syn1, Syn2, Tb1, Tb2
- 4 Day Class: Syn1, Syn2, Tb1, Tb2
- 3 Day Class: Syn1, Syn2, Tb1

Note it is also possible to include materials from the Advanced VHDL Coding for Synthesis class.
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**Intended Audience**
The numerous examples in this course make it suitable for a student with limited VHDL. The application focus of this course results in the student being ready for VHDL based ASIC or FPGA design.

**Prerequisites**
Students taking this course should have working knowledge of digital circuits and prior exposure to VHDL through experience or the course:

- **Comprehensive VHDL Introduction - 4 days**

**Follow-On Courses**
Students wishing to go beyond what they learned in this course should take:

- **Advanced VHDL for Synthesis and Verification – 3-5 days**

**Training Approach**
This hands-on, how-to course is taught by experienced hardware designers using a computer driven projector. We prefer and encourage student and instructor interaction. Questions are welcome. Bring problematic code.

**Contact**
To schedule a class or for more information, contact:

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