

SynthWorksSM

VHDL Training Experts



Why Get VHDL Training?

Our VHDL training helps students gain the knowledge and experience required for success. Students learn VHDL coding techniques that would otherwise take several projects to learn. Our classes help you avoid the time consuming, and hence costly, trial and error method of learning VHDL. Your return on the investment will be the completion of projects in a timely and efficient manner.

SynthWorks provides hands-on, how-to VHDL training with a focus on hardware design and verification

Why SynthWorks?

We are designers at heart. We teach VHDL syntax and coding techniques that engineers need to effectively design and verify their next FPGA and/or ASIC. Our instructors are VHDL experts who have solved difficult design and test coding problems and can answer questions in detail. We are vendor independent and teach coding styles that are portable and effective for all EDA tools. We know the current and future direction of VHDL standards because we help write them.

Get VHDL hardware experience with our FPGA based Lab board

Our Courses (Partial Listing)

SynthWorks offers a wide range of VHDL classes that are appropriate for either new or experienced VHDL engineers.

Comprehensive VHDL Introduction - 4 days

Learn VHDL syntax plus the basics of RTL and testbench coding
Students get hardware experience with our FPGA based lab board

VHDL Testbenches and Verification - 3 days

Learn to simplify writing tests by creating transaction-based testbenches

Intermediate VHDL Coding for Synthesis - 2 days

Learn RTL (hardware) coding styles that produce better, faster, and smaller logic

Advanced VHDL Coding for Synthesis - 2 days

Learn to avoid RTL coding issues, problem solving techniques, and advanced VHDL constructs.

We offer both on-site and public class sessions

What Our Customers Say

"Emphasized key concepts, labs drove home ideas."
"Excellent insight into unseen/unexpected gotcha's."
"Enjoyed having a designer teach the course."

www.SynthWorks.com

Learn VHDL from a Designer's Perspective with SynthWorks