Advanced VHDL Testbenches and Verification

5 Days: 50% lecture, 50 % Lab

Advanced Level

Course Overview

In Advanced VHDL Testbenches and Verification, you will learn the latest VHDL Verification techniques and methodologies for FPGAs, PLDs, and ASICs, including the Open Source VHDL Verification Methodology (OSVVM). Techniques include transaction level modeling (tlm), self-checking, scoreboards, memory modeling, functional coverage, directed, algorithmic, constrained random, and intelligent testbench test generation. You will gain the knowledge needed to improve your verification productivity and create a VHDL testbench environment that is competitive with other verification languages, such as SystemVerilog or 'e'. Our methodology works on VHDL simulators without additional licenses and are accessible to RTL engineers.

This course starts with simple testbenches and progressively increases the level of abstraction. Along the way students learn about subprogram usage, libraries, file reading and writing, modeling issues, transaction-based testbenches, bus functional models, transaction level models (tlm), record types, resolution functions, abstractions for interface connectivity, model synchronization methods, protected types, access types (pointers), data structures (linked-lists, scoreboards, memories), directed, algorithmic, constrained random, and coverage driven random test generation, self-checking (result, timing, protocol checking and error injection), functional coverage, representation of analog values and periodic waveforms (such as triangle or sine waves), timing and execution of code, test planning, and configurations.

The lecture and labs in this class contain numerous examples that can be used as templates to accelerate your test and testbench development.

The final result is a system-level, transaction-based, self-checking test environment. Labs track with lecture giving students the opportunity to apply what they learn. The techniques you learn in this class give VHDL a similar capability to other popular verification languages.

OSVVM, the world leading VHDL FPGA and PLD verification methodology, was developed by SynthWorks and grew up as part of this class. Each OSVVM package was used in class prior to its release into OSVVM, some of them for years. Taking this class from us helps further support the development of OSVVM and gives you the deep insight into the methodology that is only available from its developers.

Jumpstart your verification effort by reusing OSVVM packages for transaction based modeling, constrained and Intelligent Coverage™ random testing, functional coverage, error and message handling, interprocess synchronization, scoreboards, FIFOs, and memories
VHDL Testbenches and Verification

**Intended Audience**

*Advanced VHDL Testbenches and Verification* is recommended for experienced VHDL designers who are looking to improve their verification efficiency and effectiveness.

**Course Objective**

In this class, you will learn to:
- Use OSVVM's structure transaction base framework
- Write OSVVM Verification IP
- Simplify test writing using interface transactions (CpuRead, CpuWrite)
- Add error injection to interface transactions
- Implement a test plan that maximizes reuse from RTL to core to system-level tests
- Write directed, algorithmic, constrained random, and Intelligent Coverage random tests
- Write Functional Coverage to track your test requirements (test plan)
- Simplify error reporting using OSVVM's Alert and Affirm utilities
- Simplify conditional message printing (such as for debug) using OSVVM's log utilities
- Add self-checking to tests
- Use OSVVM's Generic Scoreboards and FIFOs
- Use OSVVM's Synchronization Utilities (WaitForBarrier, WaitForClock, ...),
- Model analog values and periodic waveforms,
- Utilize OSVVM's growing library of Open Source Verification IP

**Course Outline**

**Day 1, Module TB1**
- Testbench Overview
- Basic Testbenches
- Transactions and Subprograms
- Modeling for Verification
- VHDL IO
- Labs: UartTx Using Subprograms

**Day 2, Module TB2**
- Lab Review: Testing w/ subprograms
- Transaction-Based Models (BFM)
- Elements of a Transaction-Based BFM
- Data Structures for Verification
- Labs:
  - UartTx Model (Verification IP)
  - Injecting Errors in UartTx
  - Scoreboards

**Day 3, Module TB3**
- Lab Review: UartTx BFM
- Creating Tests
- Constrained Random Testing
- Functional Coverage

**Day 4, Module TB4**
- Execution and Timing
- Configurations and Simulation Management
- Advanced Coverage
- Advanced Randomization
- Labs:
  - Core Testing
  - Configurations

**Day 5, Module TB5**
- Lab Review: Scoreboards, Randomization and Coverage
- Test Plans
- Modeling RAM

**Going Further**
- Transaction-Based BFM Part 2

Learn VHDL from a designer's perspective with SynthWorks.
VHDL Testbenches and Verification

Prerequisites
Students taking this course should have working knowledge of digital circuits and prior exposure to VHDL through experience or the course:

Comprehensive VHDL Introduction - 4 days

Other Recommended Courses
Students may also be interested in the following companion course:

VHDL Coding for Synthesis - 4 days

Details
This class is a 5-day journey into VHDL coding styles, techniques, and methodologies that will help you become more productive at design verification and testbenches.

The heart this approach is transaction-based testing. Transaction-based testing abstractly represents an the interface operation, such as a CPU read, CPU write, UART transmit or UART receive. In this class we learn two forms of transaction-based testbenches: a simple subprogram based approach, and a more capable bus functional model based approach. Both approaches use subprograms to initiate a transaction. A single test is a sequence of subprogram calls. A suite of tests is a collection of VHDL architectures. Using transaction calls makes tests easier to write and read, and more tests can be written in less time. The subprograms are created in a package, allowing them to be reused by all testbenches. Additional subprograms are used to encapsulate commonly used sequences of transactions (such as initialize UART and start DMA) further improving effectiveness of writing and reading tests. While either the subprogram implementation or the transaction model may change between subblock, core, and system-level tests, the subprogram call interface largely remains unchanged allowing many tests and test models to be reused or pre-used at each of these levels - further improving your efficiency. To simplify using records as an interface channel, SynthWorks provides a resolution package as open source.

Another important topic is test generation. In class we learn how to create directed, algorithmic, constrained random, and Intelligent Coverage random tests. Using these methods, students learn how create tests that model a CPU, UART, FIFO, memory, arithmetic, and analog designs. Since transactions are the basis for these tests, it is easy mix any of the techniques together. This means that if a directed or algorithmic sequence can achieve test coverage faster, it can be used either by itself or mixed in with the randomization methods. The randomization and functional coverage packages that provide the foundation for constrained random and Intelligent Coverage random verification were released by SynthWorks into the OSVVM library.

Since manually checking a test is tedious, error prone, and time consuming, making tests self-checking is important. In class we examine a number of different means of self-checking including result checking, protocol checking, timing checks, and error injection. The scoreboard data structure used in the class, and provided as a reusable package, is a FIFO like data structure used to facilitate result checking.
VHDL Testbenches and Verification

Coverage tells us when a test is done. There are several forms of coverage including structural (code coverage) and functional. Structural or code coverage is coverage detected and reported by a simulator and is explored briefly in lecture and more detail in lab. Functional coverage goes beyond code coverage by looking for specific values or conditions to occur on an object or set of objects. The class covers functional coverage in detail and facilitates implementing it using the OSVVM coverage package (which was developed by SynthWorks).

Design verification requires a good test plan. We learn to write test plans that reuse interface waveforms, bus functional models, and test cases at the RTL, core, and system levels. Reuse removes redundancy in the verification effort and reduces the amount of time the project takes.

The SynthWorks testbench methodology uses the natural concurrency built into VHDL. Processes and models are used to create separate threads of execution for items that naturally run independently. When modeling statemachines in this approach, they can either be modeled concurrently, just like RTL code, or sequentially, just like software and OO approaches. To synchronize the separate processes, we use a synchronization primitive from a "library" of primitives contained in our open source utility package. The structure of the testbench is created with structural code just like RTL code. Compare this to other verification languages which rely on a complicated OO approach with "fork and join" to kludge in concurrency and methods for emulating elaboration and initialization that is already built into VHDL.

Customization

All of our courses can be customized to meet your specific needs. Either see our website or contact us for details.

Training Approach

This hands-on, how-to course is taught by experienced verification engineers using a computer driven projector. We prefer and encourage student and instructor interaction. Questions are welcome. Bring problematic code.

Contact

To schedule a class or for more information, contact:

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Learn VHDL from a designer's perspective with SynthWorks.